Verilog codes for SPI Protocol

(<https://www.edaplayground.com/x/5inW>) link for Verilog code

Codes for testbench

// Code your testbench here

module shftreg\_tb();

reg [7:0] din;

wire miso,dout;

reg sclk,rstn,cs,load\_en,mosi;

assign mosi = miso;

//instantiation of module shiftregister

shftreg i\_shftreg(sclk,rstn,load\_en,mosi,miso,cs,din,dout);

//clockpulse

initial begin

sclk = 0;

load\_en = 0;

#0 load\_en = 1;

#15 load\_en = 0;

end

initial begin

cs = 1;

#3 cs = 0;

end

initial begin

rstn = 0;

#5 rstn = 1;

#100 $finish;

end

always

#5 sclk = ~sclk;

//initialization of input

initial begin

din = 8'b10110011;

end

initial begin

$dumpfile("dump.vcd");

$dumpvars;

end

endmodule

Code For DUT

// Code your design here

module shftreg(sclk,rstn,load\_en,mosi,miso,cs,din,dout);

input sclk,rstn,load\_en,cs;

input reg mosi;

input [7:0] din;

reg [7:0] dint;

output reg miso;

output reg [7:0] dout;

//wire a , b;

//assign a = sclk & (~cs);

//assign b = mosi & ( ~cs);

////////////////////////////////////////////////////

always @(negedge sclk or negedge rstn)

begin

if(~rstn)

dint <= 8'h00;

else if(load\_en)

dint <= din;

else

dint <= dint << 1;

end

///////////////////////////////////////////////

assign miso = dint[7];

always @(posedge sclk or negedge rstn)

begin

if(~rstn)

dout <= 8'h00;

else

begin

dout[0] <= mosi;

dout[7:1] <= dout[6:0];

end

end

endmodule